

# Fighting Guide **PIC64**<sup>™</sup> **GX**

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## Competitive Positioning

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# Competitive Overview

**PIC64GX competes against other quad core processors**

- NXP i.MX 8M Nano and Mini
- TI Sitara
- Renesas RZ

**Competitors have a range of family members with different feature sets.  
Comparing apples to apples is important**

**PIC64GX is the only RISC-V based MPU in this class**

**PIC64GX has extra value depending on the application requirements**

# Positioning PIC64GX

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# PIC64GX Delivers a Differentiated Solution

	<b>PIC64<sup>™</sup> GX</b>	NXP i.MX8M Nano	Renesas RZ	TI Sitara
<b>64-bit Multicore CPU</b>	●	●	●	●
<b>Flexible Asymmetric Multi-Processing</b>	●	○	○	○
<b>Real-Time Support</b>	●	On isolated ARM CPU Only	On isolated ARM CPU Only	On isolated ARM CPU Only
<b>Embedded NVM</b>	●	○	○	○
<b>PCIe</b>	●	○	●	○
<b>2x Gigabit Ethernet</b>	●	Only 1	●	Only 1
<b>User Crypto, Secure Boot</b>	●	● AES/RSA Only	● >SHA-256	● No ECDSA
<b>Anti-tamper, DPA Resistance</b>	●	○	○	○
<b>MIPI CSI-2</b>	●	●	●	●
<b>HDMI</b>	●	MIPI DSI-2	MIPI DSI-2	MIPI DSI-2
<b>Large L2 Cache</b>	●	○	○	○
<b>x32 DDR</b>	●	○ x16	●	○ x16

# Value Drivers for PIC64GX

- **Flexible asymmetric multi-processing**
  - More flexible configuration for mixed RTOS and Linux applications
  - Large 2MB L2 Cache with deterministic operation. Faster operation.
  - Worth incremental \$5 for the right customers
- **Best-in-class security**
  - Full crypto accelerator with differential power analysis (DPA) to counter physical side channel attacks. Invaluable security beyond secure boot.
- **Embedded non-volatile memory**
  - 128KB for boot. 56KB for secure keys and user data
  - Faster, secure boot times than from internal ROM

# Value Drivers for PIC64GX (cont.)

- **PCIe Root Port**
  - Only available in more expensive competitive devices which cost \$5-10 more
- **X32 DDR4/LPDDR4 interface**
  - Only available in more expensive competitive devices which cost \$5-10 more
- **2x 1GigE rather than 1 in the low-cost competitor devices**

# What Applications Will PIC64GX Not Address?

- PIC64GX does not have a GPU built in
  - PIC64GX does not have digital audio interfaces
  - Low-cost dual and quad core applications with no need for value add features in PIC64GX family
  - AI/ML intensive capabilities available in higher-cost MPUs like i.MX 95 or those from Nvidia
- **PIC64GX is very competitive with MPUs \$5 cheaper if needing any of the value drivers for the family**

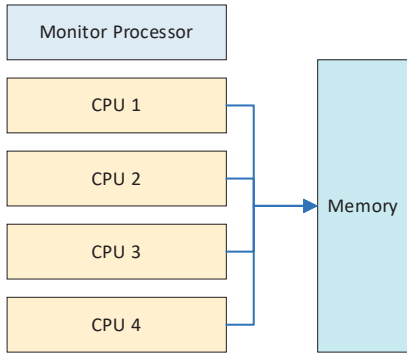
# Value Driver Details

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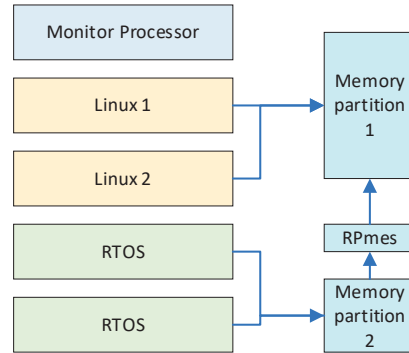


# Asymmetric Multi-Processing

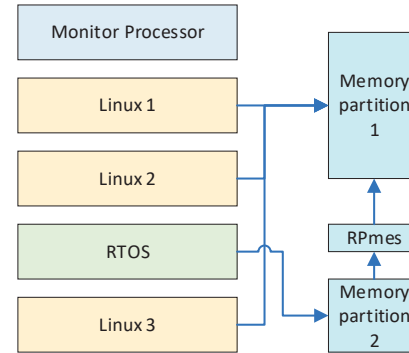
## Microchip



Symmetric Multiprocessing



PIC64GX Asymmetric Multiprocessing 1



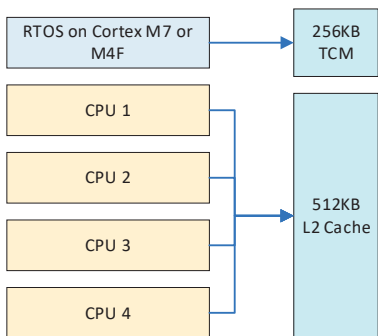
PIC64GX Asymmetric Multiprocessing 2

- Flexible configuration to 2 contexts
- 2MB L2 Cache for better deterministic MPU performance
- Physical Memory Protection



ISR Execution Is Deterministic

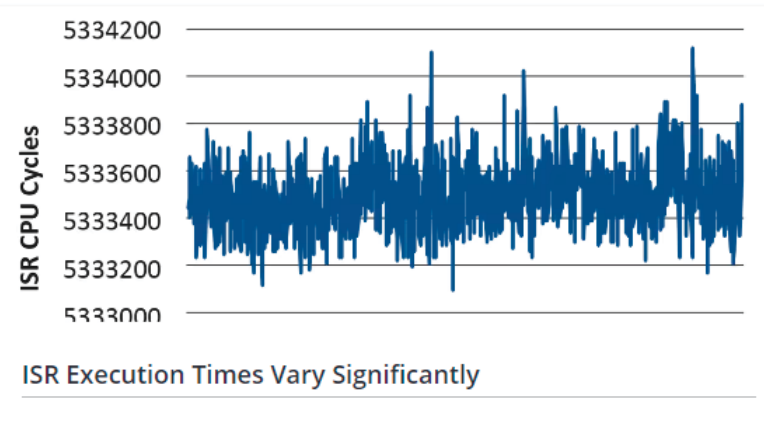
## Competition



i.MX 8M Nano and TI Sitara Multiprocessing

### Disadvantages

- Only a single context can run in the 4 application processors
- RTOS support only in the MCU class processor
- Only 512KB L2 Cache limits MPU performance



ISR Execution Times Vary Significantly



# Crypto Accelerator

- **PIC64GX Value**

- DPA resistance, tamper detection, PUF protected key storage

Features	PIC64GX	i.MX 8M Nano	TI Sitara	Renasas RZ V2H	Renasas RZ Five
AES	AES-128/192/256 (ECB, CBC, CTR, OFB, CFB, GCM, KeyWrap)	AES-D	AES-128/192/256	AES-128/192/256	AES-128/192/256
SHA	SHA-1/224/256/384/512, Key Tree	x	SHA-2/224/256/384/512	SHA-1/224/256	SHA-1/224/256
HMAC	HMAC-SHA-1/224/256/384/512; GMAC-AES; CMAC-AES	x	x	x	x
RSA	SigGen (ANSI X9.31, PKCS v1.5), SigVer (ANSI X9.31, PKCS v1.5)-1024/1536/2048/3072/4096	Supported (no specifics)	Public Key Accelerator assist of RSA/ECC	RSA 4096	RSA 4096
ECDSA	KeyGen, KeyVer, SigGen & SigVer - NIST & Brainpool (P256/384/521); KAS - ECC CDH, PKG, PKV	x	x	ECDSA256	x
FFC	KAS - DH, DSA SigGen & SigVer (1024/1536/2048/3072/4096)	x	x	x	x
Tamper Sense	Voltage, Temperature, Clock Frequency, Clock Glitch, Active Mesh	x	x	x	x
PUF	PUF protection for Secure Key storage (Secure Boot and Data communication)	x	x	x	x
DPA Resistance	DPA resistant hard crypto co-processor supporting all above Crypto algorithms	x	x	x	x